

DACS-HT – Data Acquisition and Control System for High-Temperature Applications

Kay Gorontzi¹, Reneé Lerch¹, Norbert Kordas¹, Michael Alfring¹, Mark Jung², Michael Engeln¹

¹ *Fraunhofer Institut für Mikroelektronische Schaltungen und Systeme (FHG-IMS), Finkenstraße 61, Duisburg 47057, Germany*

² *Texas Instruments Deutschland GmbH, Haggertystr. 1, Freising 85356, Germany*

Abstract

This paper presents a novell chipset for a High Temperature Data Acquisition and Control System (DACS-HT) that is comprised of five different circuits: Communication Gateway, Analog-Digital-Converter, Power-PWM, EEPROM and Pressure Sensor. All these chips, with the exception of the Pressure Sensor, are assembled on common ceramic multilayer chip module. The circuits are well suited for operating temperatures up to 250 °C and are intended to be used in a chemical microreactor system at first.

The chips are fabricated using the IMS HT-SOI CMOS technology with highly temperature-resistant tungsten metallization for improved reliability.

1. Introduction

The DACS-HT chipset was developed by the Fraunhofer Institute of Microelectronic Circuits and Systems (IMS, Germany) to answer the need for electronic measurement and control in applications that require operation at temperatures of up to 250 °C. While some of these applications allow the placement of the electronic system component securely away from the heat, there are many this is not a viable alternative due to communications, signal integrity or space constraints. Examples for such systems are oil and gas well drilling and maintenance systems, aerospace engines or, as the first application of the DACS-HT, chemical microreactor systems.

2. Overview

The basis of the DACS-HT is a chip set comprising five chips fabricated using the IMS HT-SOI CMOS technology. This high temperature silicon on insulator technology leverages the low leakage currents of SOI to extend the useful operating range of CMOS circuits to 250 °C and above, and improves circuit reliability through the use of a highly temperature-resistant tungsten interconnect.

Even the initial application, chemical microreactor systems, includes a range of microreactor modules having different measurement and control requirements. The chip set was developed to address these measurement and control needs through a hierarchical bus system which allows mixing and matching the chips to the task at hand. This chip set comprises five chips: Communication Gateway, Analog-Digital-Converter (ADC), Power-PWM, EEPROM and Pressure Sensor. All these chips, with the exception of the Pressure Sensor, are assembled on common ceramic multilayer chip modules (MCM). The first version of these MCMs comprises one each of those chips, but the communication architecture allows for later variants that feature none to

four chips of each kind. The Pressure Sensor, a micro mechanical sensor integrated with signal-conditional circuits on a single chip, is mounted in a special, pressure transducing package which can be located close to the ducts carrying the medium. It is connected to the ADC through a dedicated interface.

All chips operate off a single 5 V power supply provided on the module. All signals are TTL-compatible, except for the power terminal of the PWM, which withstands voltages of up to 24 V and can sink up to 2 A of current.

3. Internal Communication

The communication inside the MCM uses a simple intra-module "local" bus, which is coupled to the inter-module "global" bus via a gateway circuit. The local bus is a variant of the popular I²C/SMB bus, with the gateway as the sole master. It uses the CRC protocol of the SMB bus to provide a high degree of data integrity. The slave interfaces of the local bus provide features like device address decoding and variable-length data transfer. Through the use of optional jumper bond connections up to four instances of a slave device can be connected to a single local bus. Only two signals, clock and data, suffice to connect a chip to the local bus. This is much more efficient than a parallel bus system, which would use more than ten of these connections.

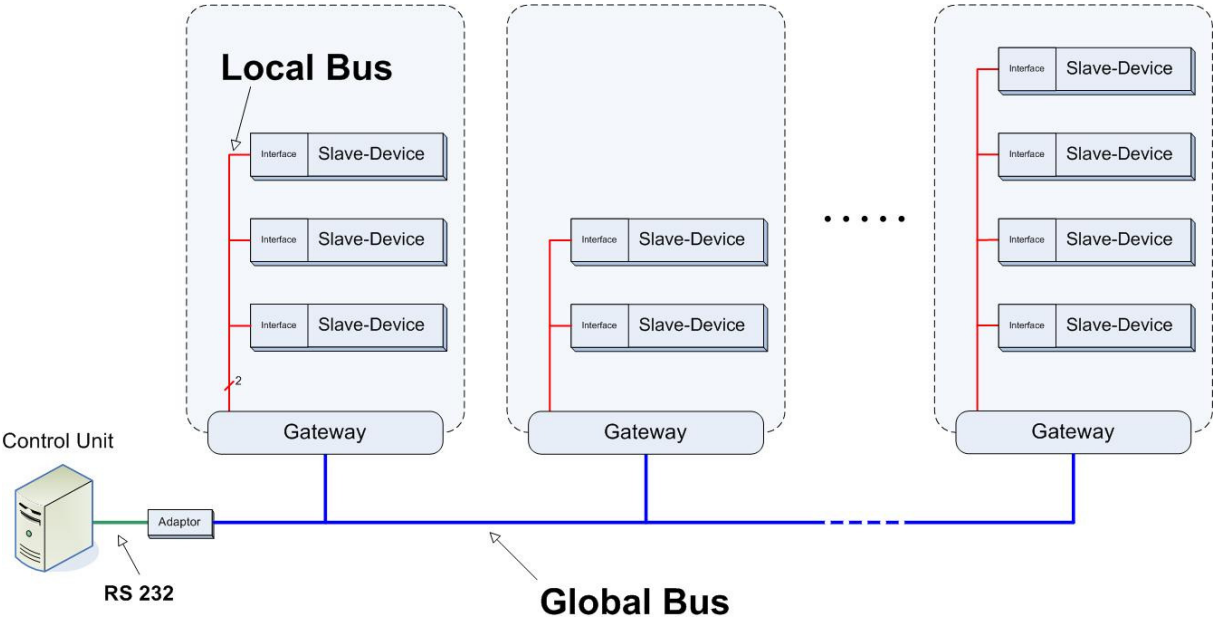


Fig. 1: Global and local communication structure

The global bus allows up to 31 MCM modules to participate. It is controlled by a central process controller, e.g. a standard desktop computer. This computer, through its asynchronous serial port and a transceiver for differential (CAN) bus levels, determines the sequence of actions on the global bus. The protocol encapsulates the I²C data for the local bus in an additional addressing and integrity control layer, so that it is open for future devices added to the local bus. The interface between global and local bus is the Communication Gateway, which decodes the global bus protocol and, if addressed, transfers the encapsulated I²C data to the global bus and back. In addition, the gateway reports the status of the module to the central process controller, either in reply to a global bus data telegram, or by activating a global alarm signal. The global

alarm signal can be activated by any module at any time to alert the process controller to unusual, possibly dangerous events, e.g. an out-of-bounds condition detected by the ADC.

4. The Communication Gateway

The global bus is coupled to the local bus via a gateway chip. This chip decodes the data telegrams on the global bus: it recognizes the synchronization sequence, compares the module address with the received address, and checks the CRC checksums. If addresses and checksums match, it conveys the embedded I2C information to the local bus, acting as the bus master. It returns the module status and all data received on the local bus to the process controller at the end of the global bus transaction.

The data transmission rate on the global bus may be set to fixed values of 115.2, 230.4 or 460.8 kBaud, or it can also be determined automatically. In the latter case transmission rates of 1.2 to 460.8 kBaud are supported. The transmission rate on the local bus is 131.7, 263.3, 395.0 or 526.6 kBaud, automatically selected to be greater than the transmission rate of the global bus. The global bus address may also be set to a fixed value, but there is also support for an address resolution protocol to assign a dynamic address.

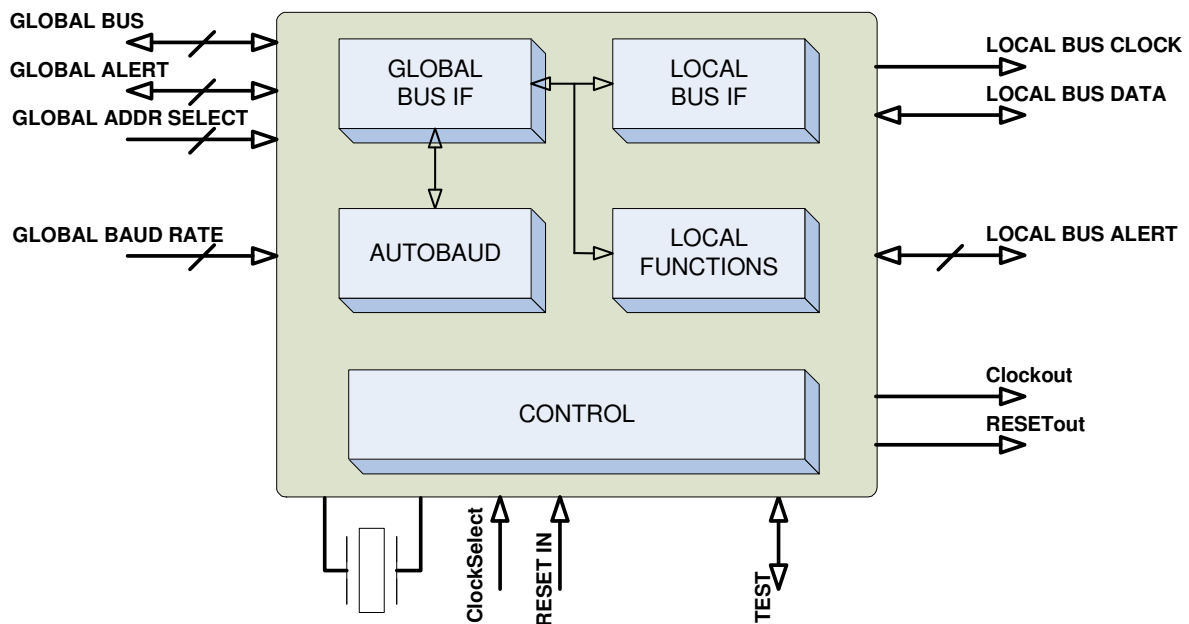


Fig. 2: Functional Communication Gateway schematic

In addition to the gateway functions the chip also provides further functions for the MCM. The programmable watchdog can reset the MCM and raise the global alert, thus providing a mechanism to recover from a "hanging" gateway. Four programmable I/O pins can act as level- or edge-sensitive inputs, whose state is reported in the module status that is transmitted at the end of each global bus transaction, or as programmable outputs. A quartz oscillator and power-on-reset circuits generate clock and reset signals, and drivers distribute them to up to 10 chips on the MCM. Fig. 2 shows a photograph of the the manufactured gateway chip.

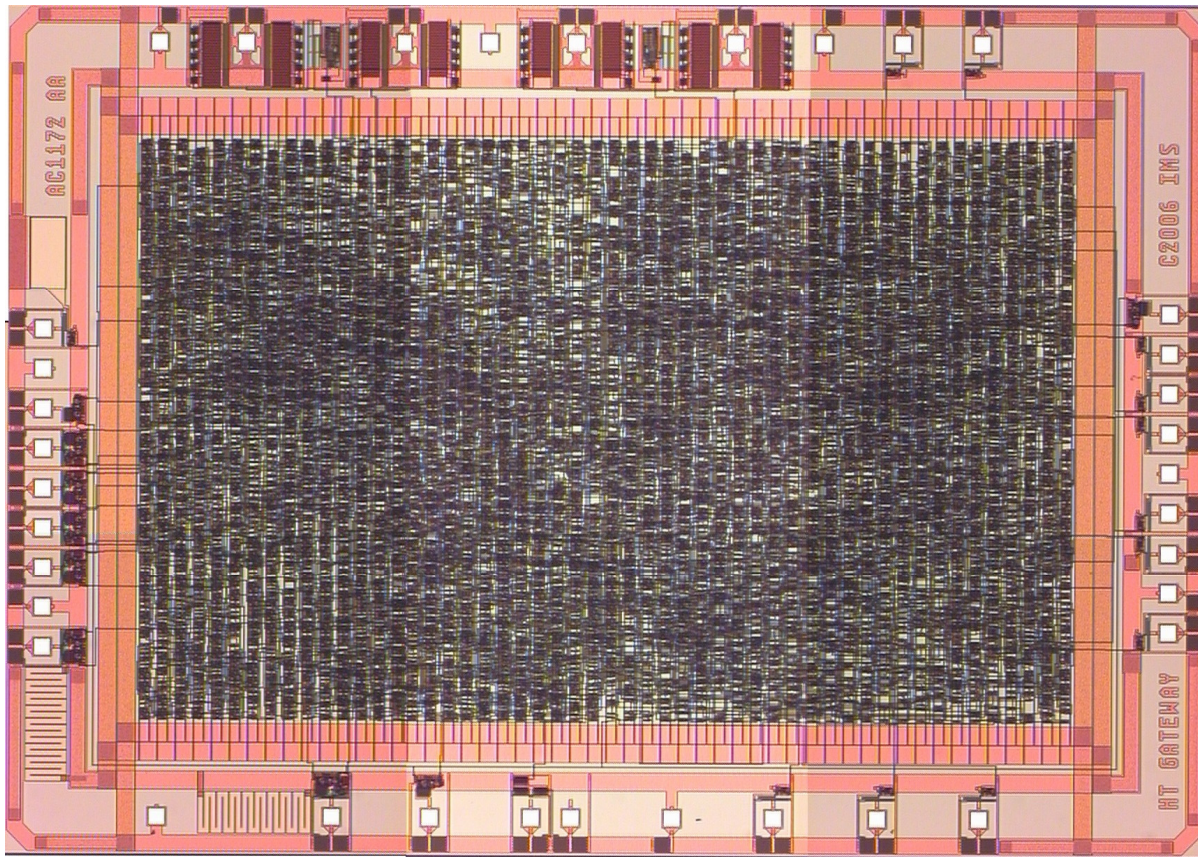


Fig. 3: Communication Gateway die photograph

The shown communication gateway covers a chip area of 31 mm².

5. EEPROM

The EEPROM chip is used to store information specific to the MCM it is mounted in. This information can be a simple identification number or calibration data needed for the sensors incorporated in the module. A total of 128 bytes of information is available for these purposes. The access to the data, status information and test modes is provided by the local bus interface. Up to 4 EEPROMs may be present to a single Communication Gateway.

The use of EEPROM as a non-volatile memory in a high temperature environment faces the challenge of reduced retention time at elevated temperatures. This challenge is met by special EEPROM circuit topologies alleviating this effect. In addition, a single-error correction and double error detection redundancy coding provides an early warning of data loss, thus permitting the implementation of data refresh by the system designer. This refresh-on-demand method reduces the number of programming cycles and thus significantly increases the life time of the EEPROM storage cell.

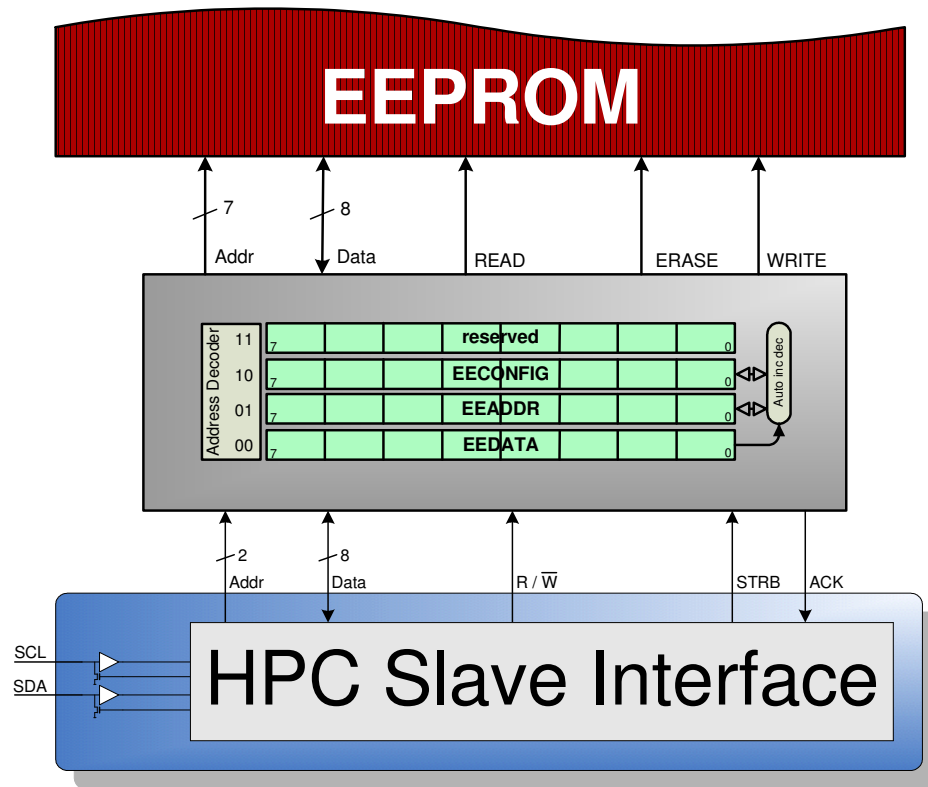


Fig. 4: EEPROM Interface

A photograph of the EEPROM is shown below in Fig. 5. The digital I²C bus interface can easily be identified on the left side while the memory matrix cells are located at the right half of the chip. The total chip size is about 14 mm².

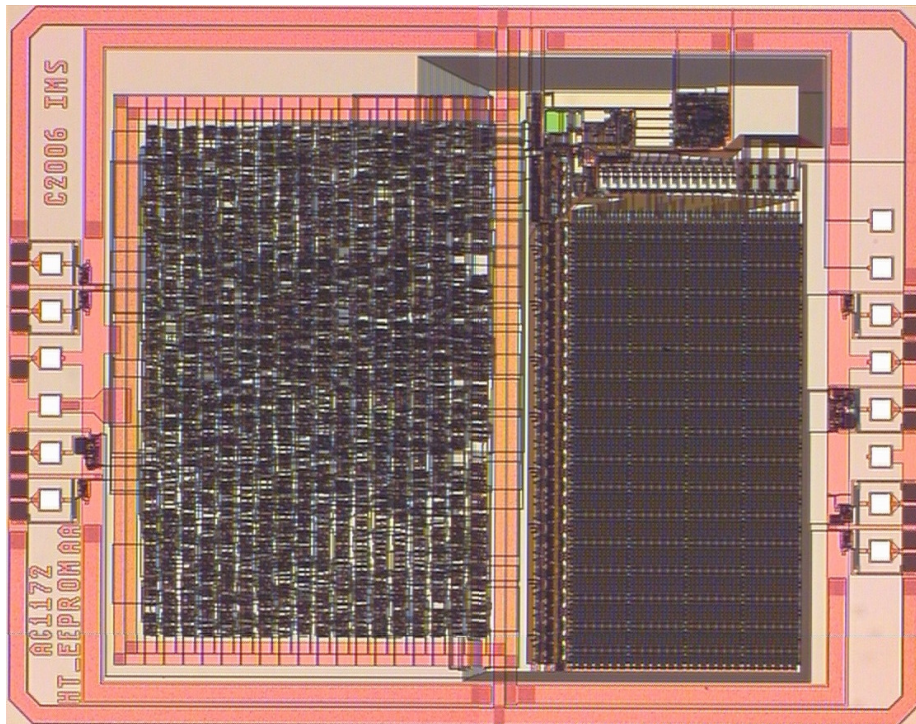


Fig. 5: EEPROM photograph

6. Analog-Digital-Converter

The ADC provides up to 8 measurement results, which may originate from the 8 analog signal inputs, or from the special interface to the Pressure Sensor. Any mix of these signal sources is supported. The ADC core is realized as an algorithmic converter using the RSD principle, using a switched-capacitor filter implementation. It provides a 1 kHz sample rate with 12 bit of resolution. The ADC device can be programmed so that any two of the converted values is compared to a programmable threshold value. The state of the comparisons is made available at two device outputs, which can be used for local control in the module, or can be provided to the Communication Gateway's programmable IO for reporting to the central controller. Up to four ADC circuits can reside on a single local bus.

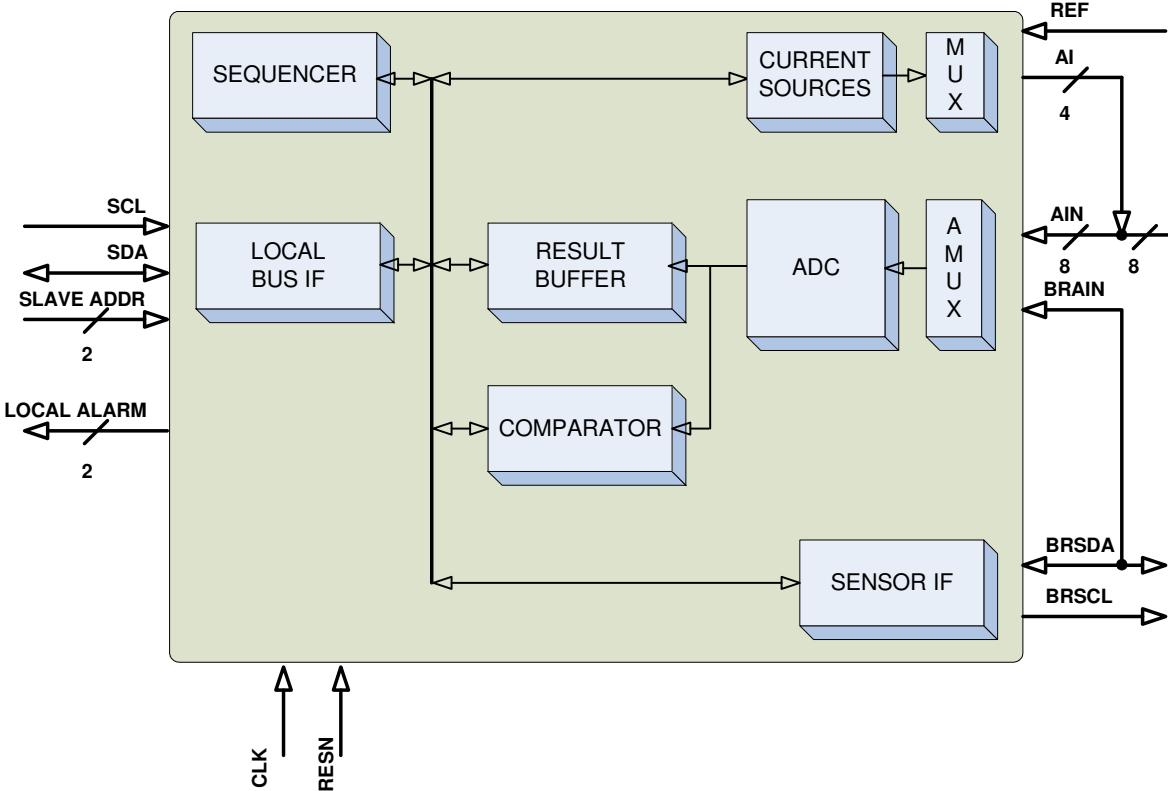


Fig. 6: Functional ADC Schematic

For four of the eight analog input signal corresponding current output ports are provided. They serve as current sources for resistive sensors, and are only active if the corresponding analog signal input is active, too. They allow ratiometric measurements of resistances, using one or more of the attached resistors as reference elements. E.g., by using two reference elements, up to two Pt1000 temperature sensors can be attached to each ADC.

Up to two Pressure Sensors can be attached to a single ADC through a special multiplexed interface. This interface uses a mixed protocol similar to that of the local bus. It allows read and write calibration data of the Pressure Sensor, as well as the analog transmission of pressure and temperature signals.

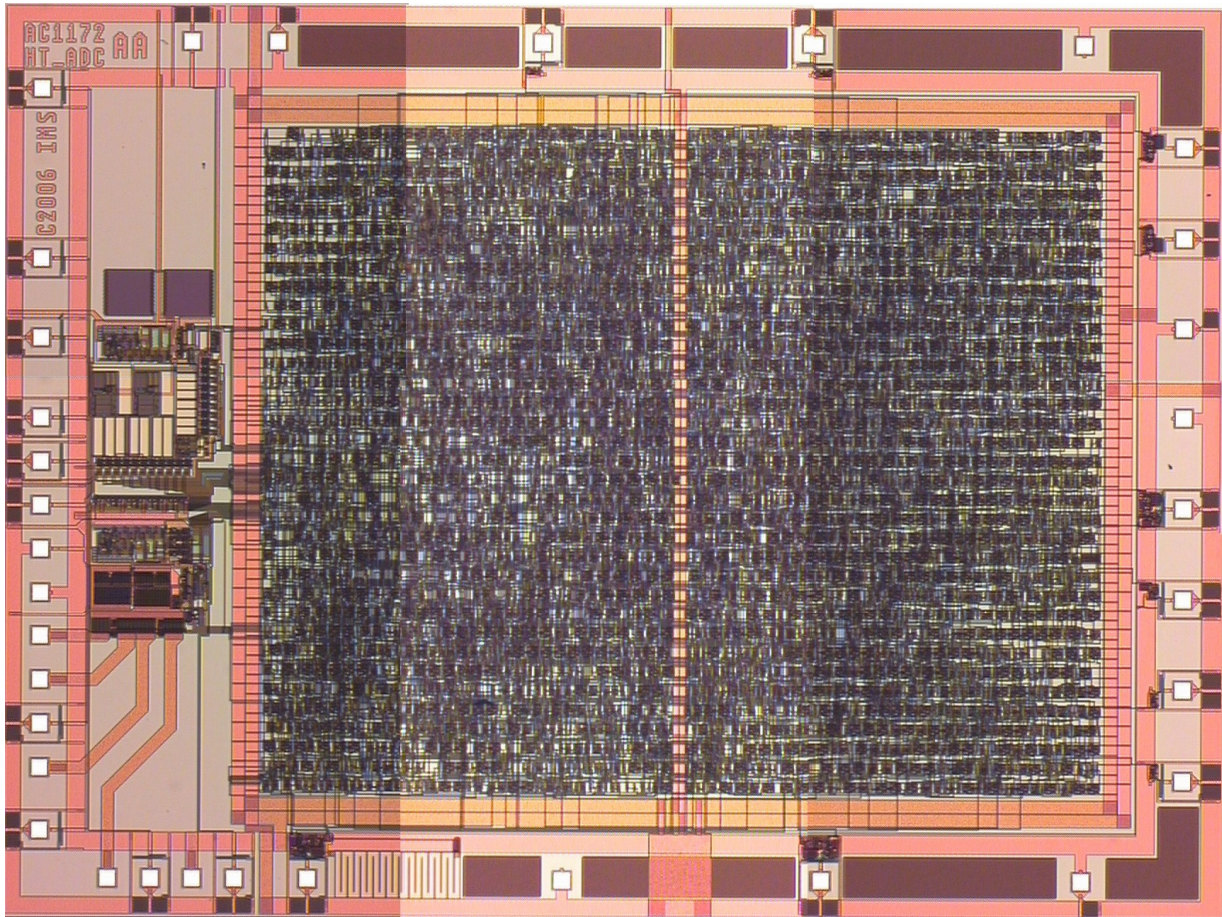


Fig. 7: ADC photograph

The ADC covers an area of 33 mm². The analog components are located at the left side and separated from the digital part. The right side comprises of the sequence control logic and the I²C bus digital interface.

7. Pressure Sensor

The Pressure Sensor consists of a micro mechanical pressure sensor, build using silicon processing techniques, and an amplification and conditioning circuit [3] on a single silicon die. This high degree of integration allows the construction of an extremely small sensor. Several versions of the sensor are available with absolute pressure ranges from 1 to above 50 bar.

The Pressure Sensor is not part of the MCM and resides in a special pressure-resistant package. Through a special interface to the ADC, the signal conditioning circuits on the Pressure Sensor chip can be programmed to amplify the signal from the micro mechanical pressure sensor and to perform a first-order linearization and temperature compensation. Up to two pressure sensors can be hooked up to each ADC.

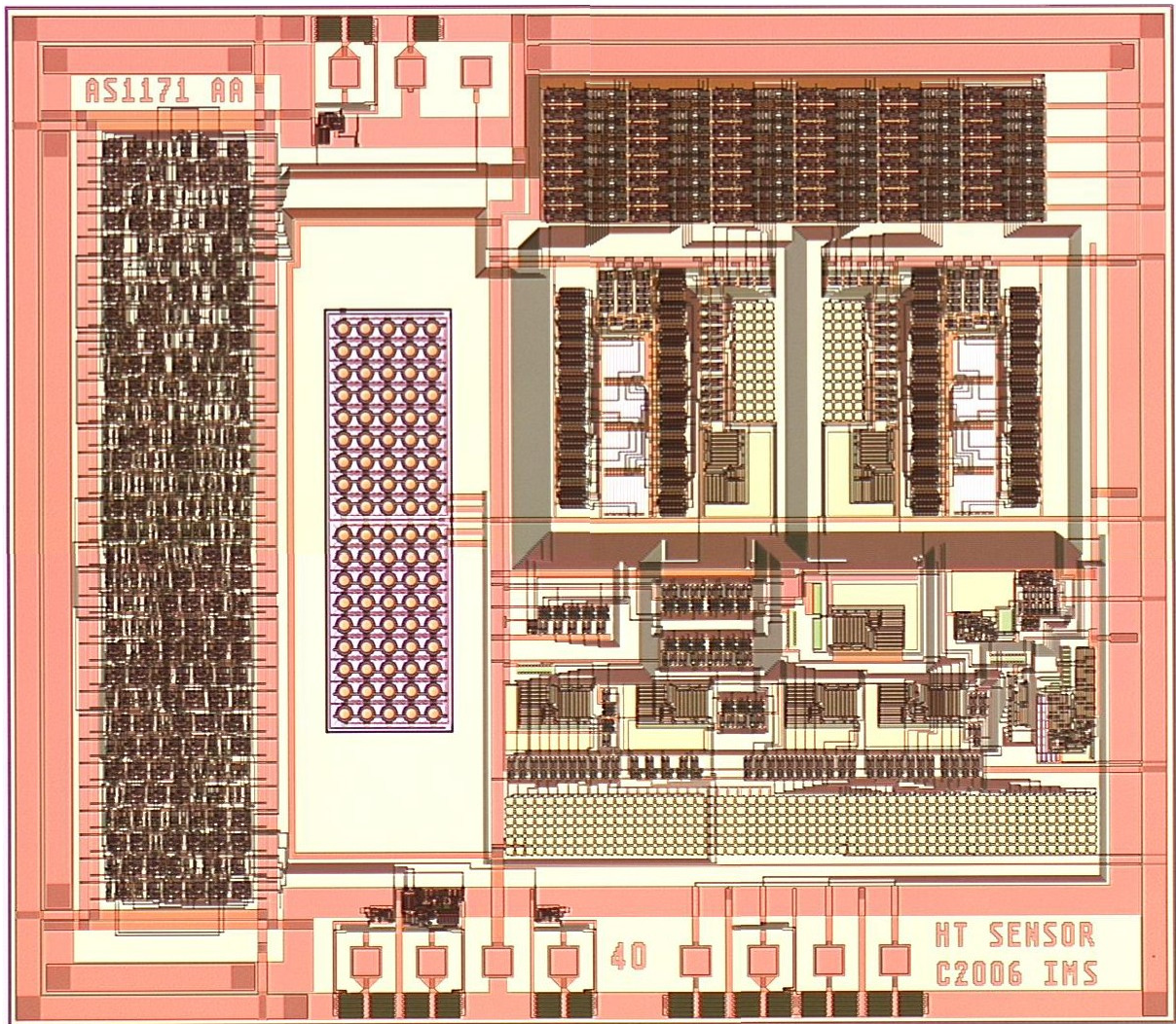


Fig. 8: Die photograph of the pressure sensor module

8. Power PWM

The Power PWM supports the generation of an analog signal with 8 bits of resolution using pulse-width modulation: within a programmable time slot, the device output is switched on for a programmable fraction of the time slot duration.

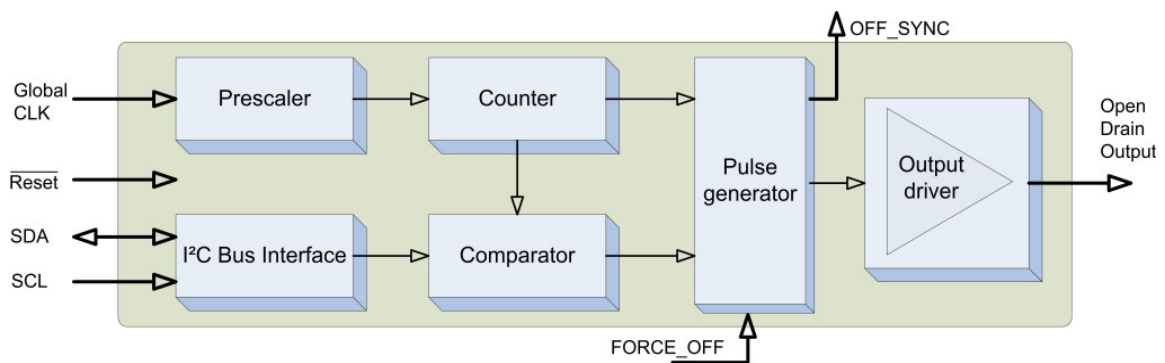


Fig. 9: Functional PWM schematic

The ratio of ON time to slot duration is proportional to the desired analog output. This mode of operation is suitable for applications like resistive heating elements. These elements can be attached to the provided open-drain NMOS output stage, which can supply 2 A of current and is rated at 24 V DC. The time slot duration and fraction values are configured through the local bus interface. Up to eight PWM chips may be connected to a single local bus.

The OFF_SYNC signal is intended to be connected to the ADC to reduce switching related signal distortions.

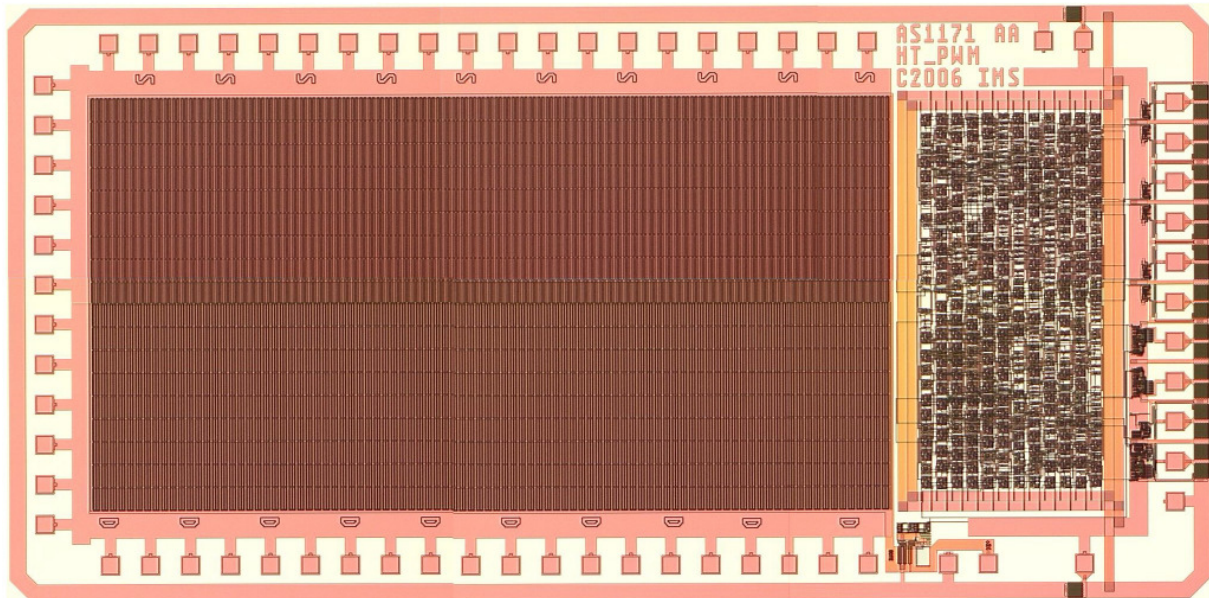


Fig. 10: Die photograph of the PowerPWM module

The PWM chip is mostly covered by the large NMOS driver transistor. Numerous pins connect its source and drain contacts (on the top and the bottom side of the chip) to the surrounding circuit. The show chip covers an area of 22 mm².

9. Conclusion

We have presented a chipset for high temperature data acquisition and control system. The chips operate at temperatures up to 250 °C matching the requirements of their first application in a chemical microreactor system. As shown in the previous paragraphs the individual chips are sufficiently versatile to be used in many other applications as well such as oil and gas well management, geothermal energy extraction and automotive industry. As the accumulated experience with this technology drives down cost and improves reliability, many new applications can be expected to take advantage of such high-temperature electronics.

References

- [1] Gogl, Fidler, Spitz, Parmentier: *A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250 °C*, IEEE Journal of solid-state circuits, Vol. 35, No. 10, October 2000
- [2] M. Spitz, M. Alfring, D. Gogl, H.-L. Fidler, B.Parmentier: *An SOI 32 Kbit EEPROM for High-Temperature Applications up to 225 °C*, HITEN Proceedings, ISBN 0-9543455-0-9, Oslo

[3] H.-K. Trieu, N. Kordas, W. Mokwa: *Fully CMOS compatible capacitive differential pressure sensors with on-chip programmabilities and temperature compensation*, IEEE Sensors 2002. Proceedings: First IEEE International Conference on Sensors, Hyatt, Orlando, 2002